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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,919	10/15/2003	William E. Welnick	33692.03.3198	7060

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EXAMINER	
RAMPURIA, SHARAD K	
ART UNIT	PAPER NUMBER
2617	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,919	WELNICK ET AL.	
	Examiner	Art Unit	
	SHARAD RAMPURIA	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-21, are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hooper; Jeff Duwayne et al.** [US 5734980 A] in view of **Cooper, Rotem** [US 20030083064 A1].

As per claim 1, **Hooper** teaches:

A circuit (in view of the steps of Figure 2) operative to acquire a more-preferred stored system identification (SID) element comprising: memory (column 6, lines 41 to 65) containing a

roaming list that includes a plurality of stored SID elements ranked according to an order of preference (column 6, lines 52 to 54) including at least one more-preferred stored SID element and at least one less- preferred stored SID element (column 6, lines 54 to 65, the more-preferred and less-preferred SID elements are being interpreted to be any SID element that is ranked above Or below respectively one another); and

Hooper doesn't teach explicitly logic circuitry, operatively coupled to the memory, and operative to perform a first more-preferred SID acquisition sequence and then a second more-preferred SID acquisition sequence that includes repeatedly attempting acquisition of the at least one more-preferred stored SID element using a same frequency during the second more-preferred SID acquisition sequence. However, **Cooper** teaches in an analogous art, that logic circuitry, operatively coupled to the memory, and operative to perform a first more-preferred SID acquisition sequence and then a second more-preferred SID acquisition sequence that includes repeatedly attempting acquisition of the at least one more-preferred stored SID element using a same frequency during the second more-preferred SID acquisition sequence. (e.g. When MMSS 100 attempts to acquire an analog system (when in analog mode), MMSS 100 (or more specifically, analog modulation and processing circuitry 104 in combination with system determination processor 108) scans all the frequencies within a set of frequencies (for example, all frequencies in an A frequency set, or all frequencies in the B frequency set) and identifies the channel in the set that has the strongest energy and the channel that has the second strongest energy. MMSS 100 then tunes to the frequency channel having the strongest energy and attempts to demodulate a received signal. If demodulation of the signal over the strongest frequency channel is not successful, then MMSS 100 tunes to the second strongest frequency

channel and attempts to demodulate a signal received on that frequency. If demodulation is successful, then the signal is said to be acquired. Once a signal is successfully acquired, then MMSS 100 detects the SID associated with the signal that was acquired; ¶ 0039) Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to including logic circuitry, operatively coupled to the memory, and operative to perform a first more-preferred SID acquisition sequence and then a second more-preferred SID acquisition sequence that includes repeatedly attempting acquisition of the at least one more-preferred stored SID element using a same frequency during the second more-preferred SID acquisition sequence in order to provide a method to improve the way subscriber stations attempt to acquire (including, re-acquire) systems.

Hooper also discloses all the elements of claims 2, 7, and 11, including wherein the logic circuitry is operative to attempt acquisition of the at least one less-preferred stored SID element as part of performing the second more-preferred SID acquisition sequence. See, column 9, lines 12 to 28 and Figure 2.

Hooper also discloses all the elements/steps of claims 3, 12, and 17, including wherein the logic circuitry is operative to perform the second more-preferred SID acquisition sequence if the more-preferred stored SID element is not acquired during the first more-preferred SID acquisition sequence. See, column 10, line 65 to column 11, line 13 and Figure 2.

Hooper also discloses all the elements of claim 4, including, wherein the logic circuitry is operative to attempt acquisition by comparing received broadcast SID information with one of the plurality of stored SID elements ranked according to an order of preference including at least one more-preferred stored SID element and at least one less-preferred stored SID element. See, column 9, lines 1 to 11 and claim 1.

As per claims 5 and 13, **Hooper** teaches all the particulars of the claim except wherein the roaming list includes a first more-preferred stored SID element, a second more-preferred stored SID element, and a plurality of less preferred SID elements wherein logic circuitry is operative to perform the $secon_d$ more-preferred SID acquisition sequence, that includes repeatedly attempting acquisition of the first more-preferred stored SID element, repeatedly attempting acquisition of the second more-preferred stored SID element and a single acquisition attempt of each of the at least one less-preferred stored SID element. However, **Cooper** teaches in an analogous art, that the method of claim 1, wherein the roaming list includes a (storing) first more-preferred stored SID element, (storing) a second more-preferred stored SID element, and a plurality of less preferred SID elements wherein logic circuitry is operative to perform the $secon_d$ more-preferred SID acquisition sequence, that includes repeatedly attempting acquisition of the first more-preferred stored SID element, repeatedly attempting acquisition of the second more-preferred stored SID element and a single acquisition attempt of each of the at least one less-preferred stored SID element. (e.g. When MMSS 100 attempts to acquire an analog system (when in analog mode), MMSS 100 (or more specifically, analog modulation and processing circuitry 104 in combination with system determination processor 108) scans all the frequencies

within a set of frequencies (for example, all frequencies in an A frequency set, or all frequencies in the B frequency set) and identifies the channel in the set that has the strongest energy and the channel that has the second strongest energy. MMSS 100 then tunes to the frequency channel having the strongest energy and attempts to demodulate a received signal. If demodulation of the signal over the strongest frequency channel is not successful, then MMSS 100 tunes to the second strongest frequency channel and attempts to demodulate a signal received on that frequency. If demodulation is successful, then the signal is said to be acquired. Once a signal is successfully acquired, then MMSS 100 detects the SID associated with the signal that was acquired; ¶ 0039) Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to including wherein the roaming list includes a first more-preferred stored SID element, a second more-preferred stored SID element, and a plurality of less preferred SID elements wherein logic circuitry is operative to perform the secon$_d$ more-preferred SID acquisition sequence, that includes repeatedly attempting acquisition of the first more-preferred stored SID element, repeatedly attempting acquisition of the second more-preferred stored SID element and a single acquisition attempt of each of the at least one less-preferred stored SID element in order to provide a method to improve the way subscriber stations attempt to acquire (including, re-acquire) systems.

Hooper also discloses all the elements of claim 9, including the logic circuitry camps on at least one less-preferred stored SID element if acquisition on the at least one less-preferred stored SID element is available (column 10, lines 47 to 64) and if acquisition on the at least one more-preferred store SID element is unavailable (Id.), and wherein the logic circuitry camps on

the at least one more-preferred SID stored element if the at least one more-preferred stored SID element is acquired at any time (column 10, line 65 to column 11 line 13).

Hooper discloses all the steps of claim 15, including, receiving broadcast SID information, wherein attempting acquisition is based on comparing the received broadcast SID information with one of the Plurality of stored SID elements. See, column 9, lines 1 to 11. Hooper also discloses all the steps of claim 18, including attempting acquisition of the at least one less-preferred stored SID element as part of performing the second more-preferred SID acquisition sequence. See, column 9, lines 12 to 28.

Hooper also discloses all the elements of claim 20, including camping on the at least one more-preferred stored SID element if acquisition of the at least one more-preferred stored SID element is available (column 9, lines 1 to 11); and camping on the at least one less-preferred stored SID element if acquisition of the at least one less-preferred stored SID element is available and if acquisition of the at least one more-preferred stored SID element is unavailable (column 10, lines 47 to 64).

Hooper also discloses all the elements of claim 16. See the rejection of claims 9 and 20. Hooper also discloses all the elements of dependent claim 21, including wherein the more-preferred stored SID element defines the home system. See, step 78. of Fig.2.

Claims 6, 8, 10, 14, 19, are the wireless device, memory containing instructions executable by one or more processing devices, method claims, corresponding to the logic circuitry claim 1 respectively, and rejected under the same rational set forth in connection with the rejection of claim 1 respectively, above.

Response to Amendments & Remarks

Applicant's arguments with respect to claims 1-21, have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sharad Rampuria whose telephone number is (571) 272-7870. The examiner can normally be reached on M-F. (8:30-5 EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dwayne Bost can be reached on (571) 272-7023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sharad Rampuria/
Primary Examiner
Art Unit 2617